Abstract

A novel Finite Impulse Response ("FIR") filter (100) is provided with. A master/slave sample and hold architecture is employed. In this architecture, an input signal (V_{IN}) is coupled to an input of a master sample and hold circuit (104). At least two slave sample and hold circuits (114, 118) connect to the master output. The slave sample and hold circuits (114, 118) operate at *1/k* times the clock rate of the master sample and hold circuit (104), where *k* equals the number of slave sample and hold circuits (114, 118). A first multiplexer (126) multiplexes the slave outputs together. At least one tap block (129, 179, 207) is coupled to the first multiplexer (126) includes a multiplier (132, 180, 210), a summer (142, 142, 216), at least two slave sample and hold circuits (152, 154, 188, 190, 224, 226) and a second multiplexer (164, 200, 236). The slave sample and hold circuits (152, 154, 188, 190, 224, 226) run at *1/k* times the clock speed of the master sample and hold circuit (126).